# Single/Dual Bidirectional Multi-Voltage Level Translator for Open-Drain & Push-Pull Application

**Check for Samples: LSF0101, LSF0102**

## FEATURES

- **Provide Bidirectional Voltage Translation With No Direction Pin**
- **Less Than 1.5ns Max Propagation Delay**
- **Support High Speed Translation, Greater Than 100 MHz**
- **Allow Bidirectional Voltage Level Translation Between**
  - **1.0V ↔ 1.8/2.5/3.3/5V**
  - **1.2V ↔ 1.8/2.5/3.3/5V**
  - **1.8V ↔ 2.5/3.3/5V**
  - **2.5V ↔ 3.3/5V**
  - **3.3V ↔ 5V**
- **5V Tolerance I/O Port to Support TTL**
- **Low Ron Provides Less Signal Distortion**
- **High-impedance I/O pins For EN = Low**
- **Flow-Through Pinout for Ease PCB Trace Routing**
- **Latch-Up Performance Exceeds 100mA Per JESD 17**
- **–40°C to 125°C Operating Temperature Range**
- **Application/Interface**
  - **LSF0101: GPIO**
  - **LSF0102: MDIO, PMBus, SMBus**
- **ESD Performance Tested Per JESD 22**
  - **2000V Human-Body Model (A114-B, Class II)**
  - **200V Machine Model (A115-A)**
  - **1000V Charged-Device Model (C101)**

## DESCRIPTION

The LSF0101 and LSF0102 are bidirectional voltage level translators operational from 1.0 V to 4.5 V (Vref_A) and 1.8 V to 5.5 V (Vref_B), which allow bidirectional voltage translations between 1.0 V and 5.0 V without the need for a direction pin in open-drain or push-pull applications. The level translation application with transmission speeds greater than 100 MHz for an open-drain system with a 30 pF capacitance.

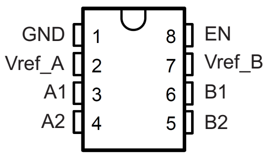
When the An or Bn port is LOW, the switch is in the ON-state and a low resistance connection exists between the An and Bn ports. The low $R_{on}$ of the switch allows connections to be made with minimal propagation delay and signal distortion. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by Vref_A. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage ($V_{pu\#}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

All channels are able to set up different supply voltage ($V_{pu\#}$) by the pull-up resistors individually. From the design-in example, Figure 2, CH1 can be used as up-translation (1.2 V ↔ 3.3 V) and CH2 as down-translation (2.5 V ↔ 1.8 V).

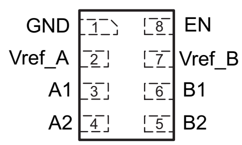
When EN is HIGH, the translator switch is on, and the An I/O is connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by Vref_B. To ensure the high-impedance state during power-up or power-down, EN must be LOW.

**LSF0102 (PREVIEW)**

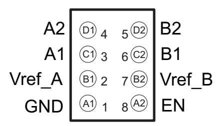
**DCT or DCU Package (TOP VIEW)**




**DQE Package (TOP VIEW)**

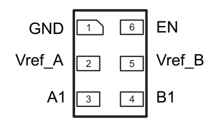



**DQE Package (TOP VIEW)**




**LSF0101**

**DRY Package (TOP VIEW)**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Function Table**

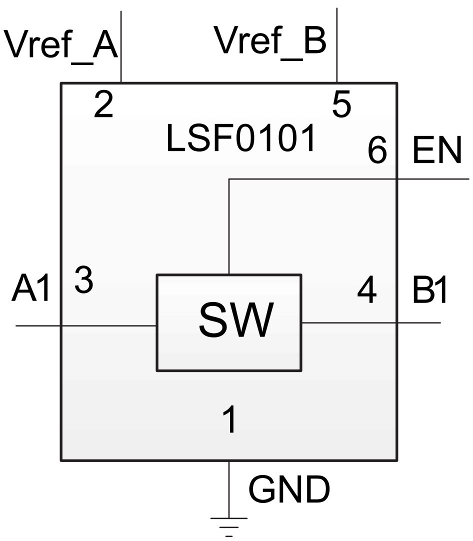
| INPUT EN(1) PIN | FUNCTION |
|---|---|
| H | An = Bn |
| L | H-Z |

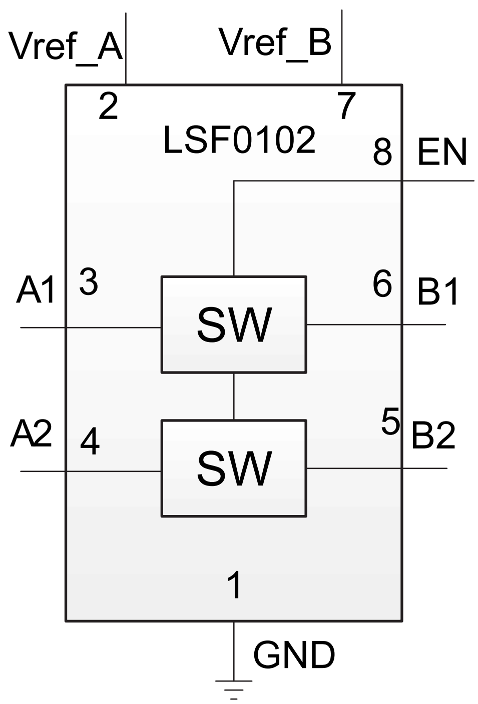
(1) EN is controlled by $V_{ref\_B}$ logic levels and should be at least 1V higher than $V_{ref\_A}$ for best translator

**Pin Functions**

| PIN | DESCRIPTION |
|---|---|
| An/Bn | Data Port |
| EN | Switch enable input; connect to Vref_B and pull-up through a high resistor (200 kΩ) |
| Vref_A | Reference supply voltage; see Application Information |
| Vref_B | Reference supply voltage; see Application Information |

## Functional Diagram



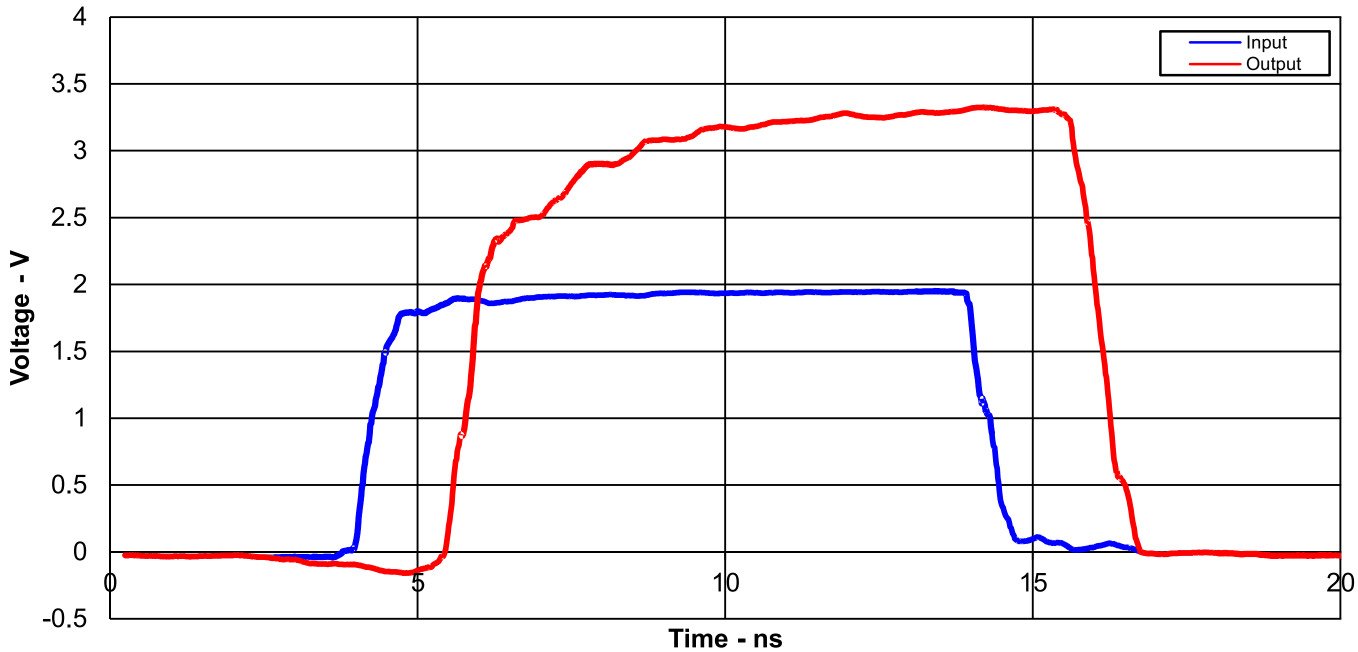



**Figure 1. Signal Integrity (1.8V to 3.3V Translation Up at 50 MHz)**

### Application Schematic

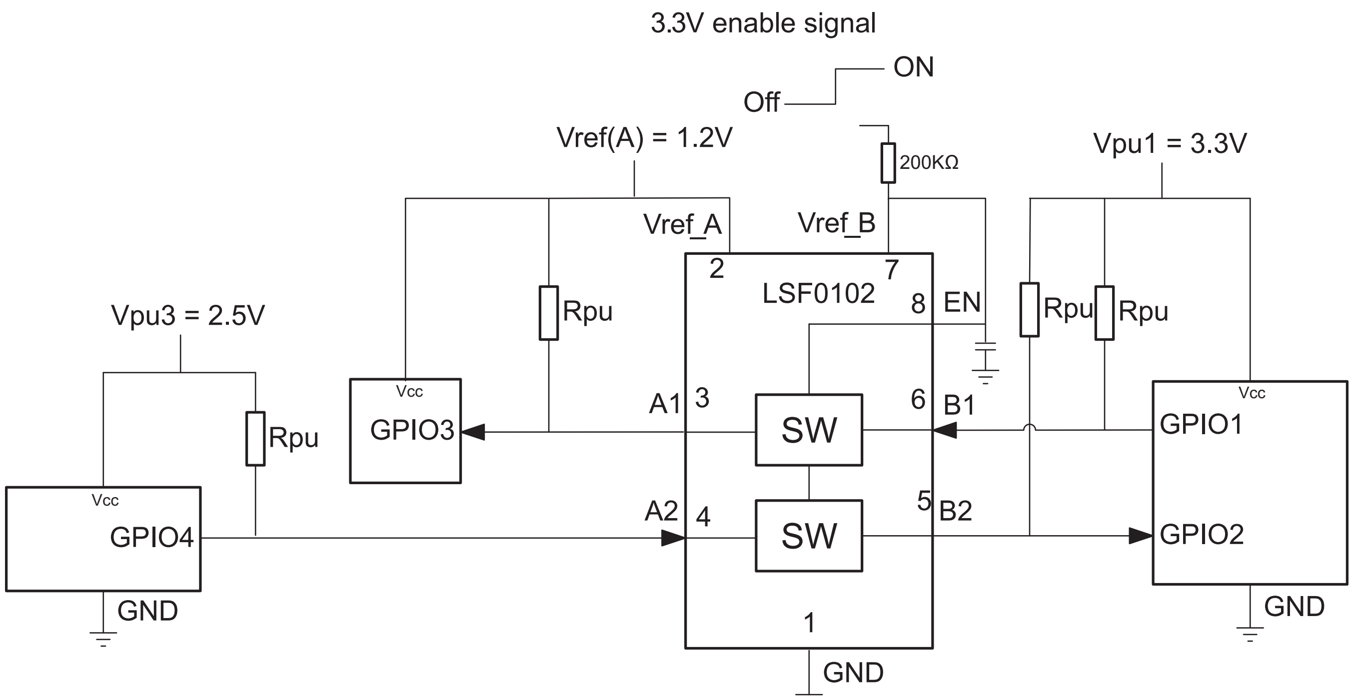



**Figure 2. Bidirectional Translation to Multiple Voltage Levels**

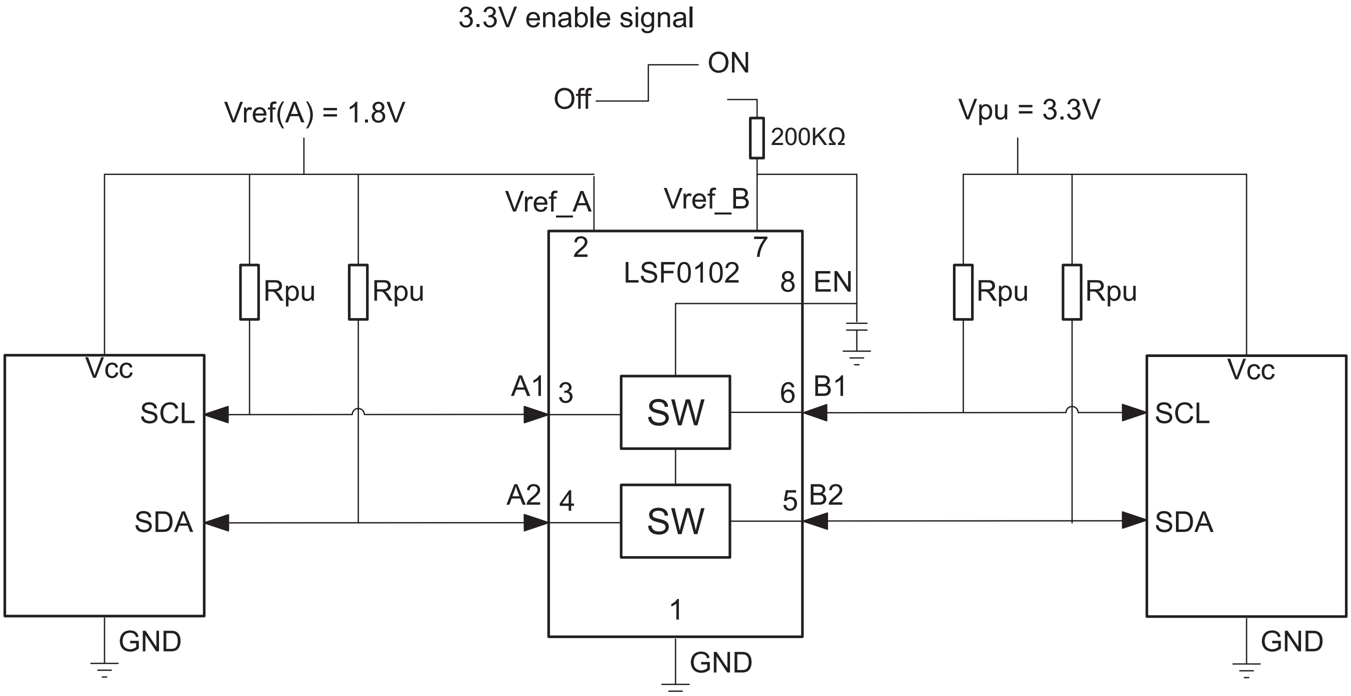



**Figure 3. Typical Application circuit (I2C Bidirectional Interface)**

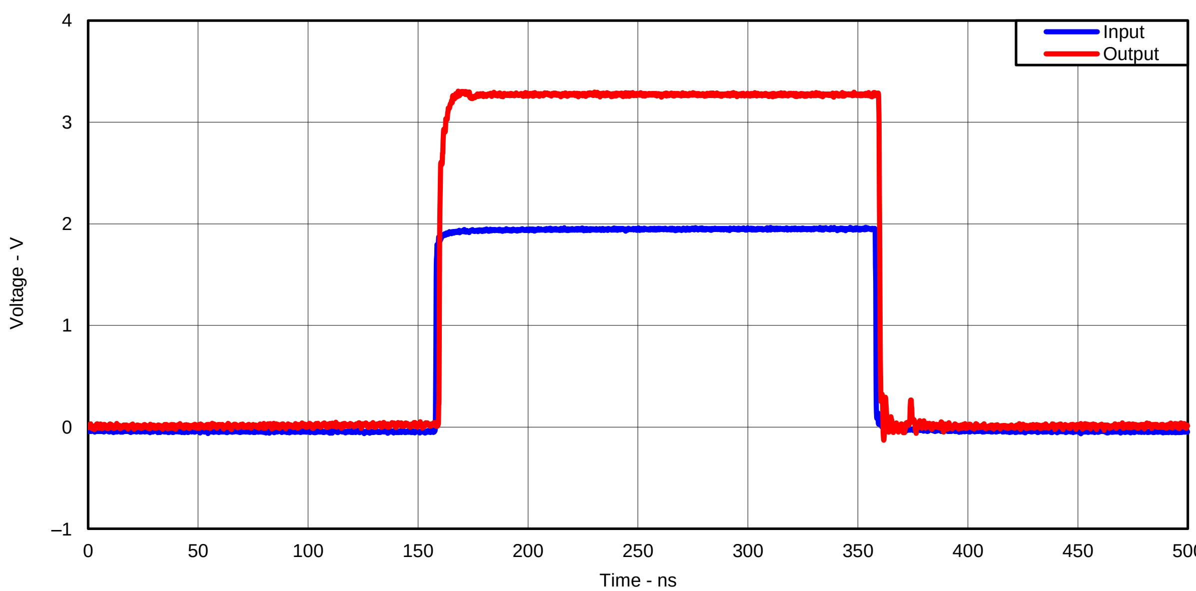



**Figure 4. Captured Waveform from above I2C set-up**

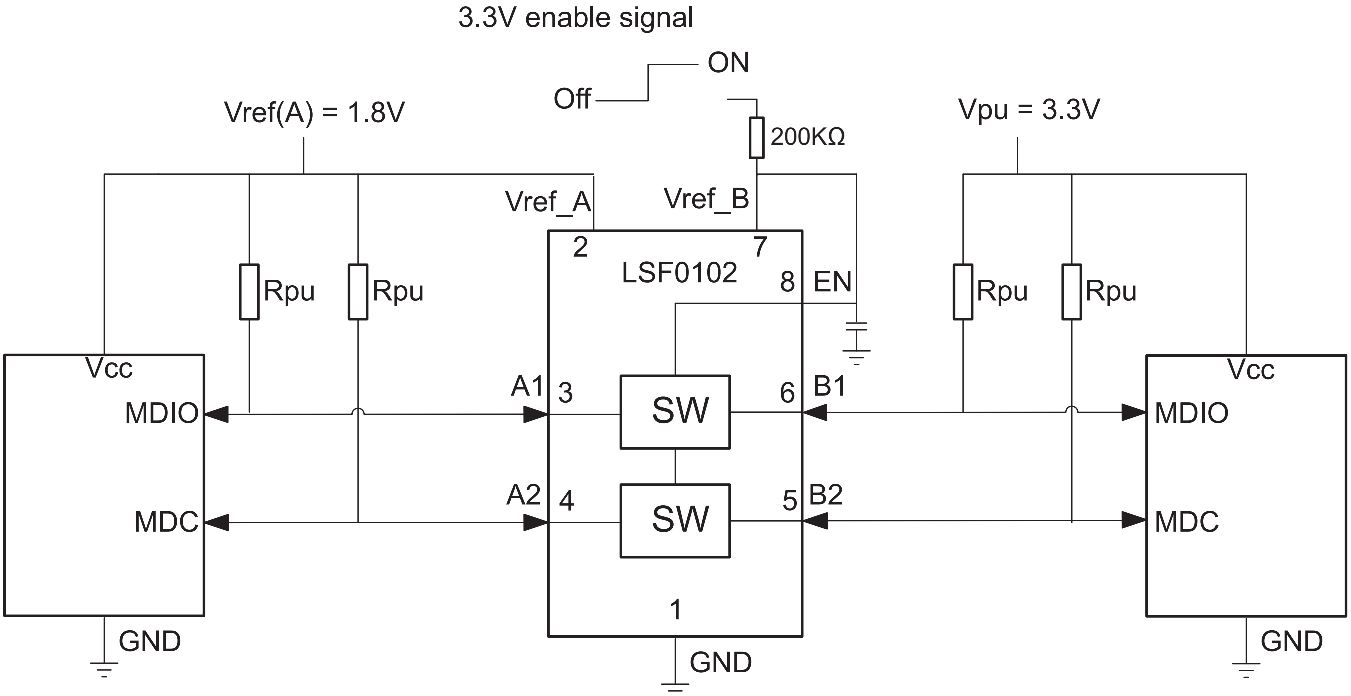



**Figure 5. Typical Application circuit (MDIO/ Bidirectional Interface)**

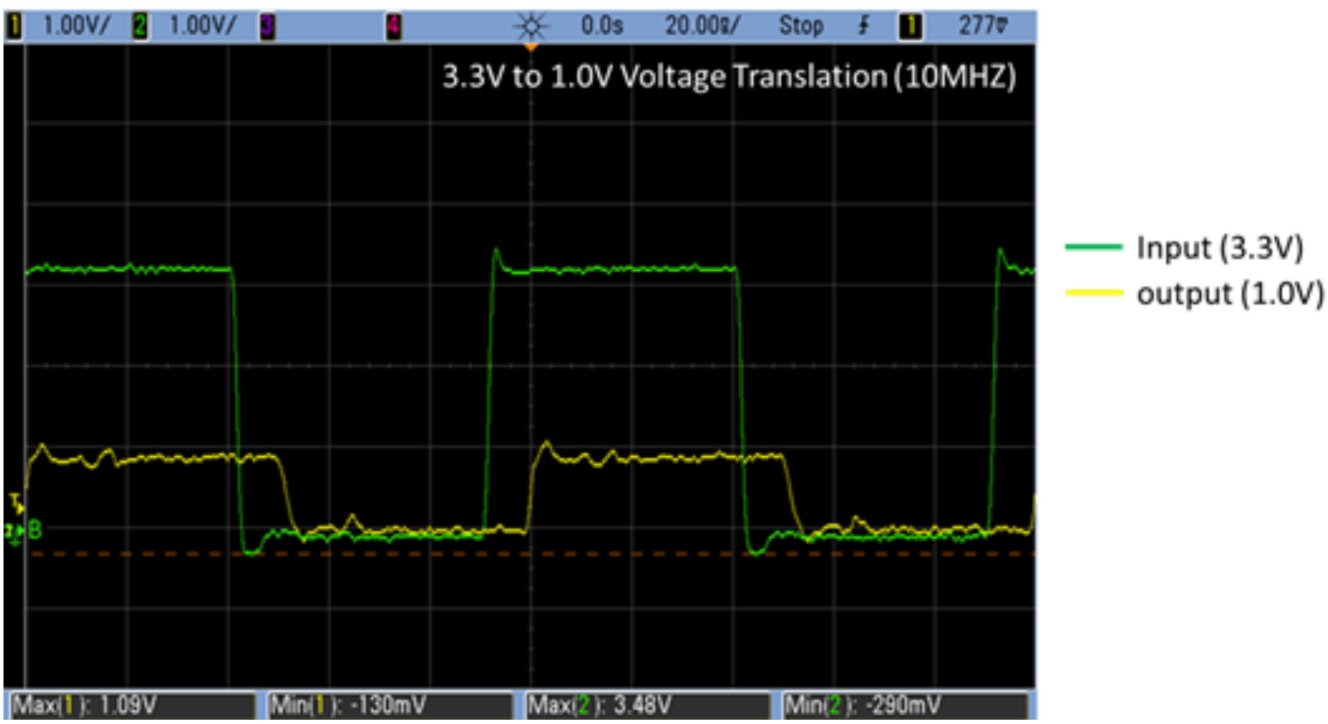



**Figure 6. Captured Waveform from above MDIO set-up**

## Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage range[2] | | –0.5 | 7 | V |
| $V_{I/O}$ | Input/output voltage range[2] | | –0.5 | 7 | V |
| | Continuous channel current | | | 128 | mA |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –50 | mA |
| $θ_{JA}$ | Package thermal impedance[3] | DCT package | | 220 | °C/W |
| | | DCU package | | 227 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{I/O}$ | Input/output voltage | 0 | | 5 | V |
| $V_{ref\_a/B/EN}$ | Reference voltage | 0 | | 5 | V |
| $I_{PASS}$ | Pass transistor current | | | 64 | mA |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $I_I$ = -18 mA, | $V_{EN}$ = 0 | | | | –1.2 | V |
| $I_{IH}$ | $V_I$ = 5 V | $V_{EN}$ = 0 | | | | 5.0 | µA |
| $I_{CC}$ | $V_{ref\_B} = V_{EN}$ = 5.5 V, $V_{ref\_A}$ = 4.5 V or 1 V, $I_O$ = 0, $V_I = V_{CC}$ or GND | | | | 1 | | µA |
| $C_{i(ref\_A/B/EN)}$ | $V_I$ = 3 V or 0 | | | | 11 | | pF |
| $C_{io(off)}$ | $V_O$ = 3 V or 0, | $V_{EN}$ = 0 | | | 4.0 | 6.0 | pF |
| $C_{io(on)}$ | $V_O$ = 3 V or 0, | $V_{EN}$ = 3 V | | | 10.5 | 12.5 | pF |
| $ro_n$[2] | $V_I$ = 0, | $I_O$ = 64 mA | $V_{ref\_A}$ = 3.3 V; $V_{ref\_B} = V_{EN}$ = 5V | | 8.0 | | Ω |
| | | | $V_{ref\_A}$ = 1.8 V; $V_{ref\_B} = V_{EN}$ = 5V | | 9.0 | | |
| | | | $V_{ref\_A}$ = 1.0 V; $V_{ref\_B} = V_{EN}$ = 5V | | 10 | | |
| | $V_I$ = 0, | $I_O$ = 32 mA | $V_{ref\_A}$ = 1.8 V; $V_{ref\_B} = V_{EN}$ = 5V | | 10 | | Ω |
| | | | $V_{ref\_A}$ = 2.5 V; $V_{ref\_B} = V_{EN}$ = 5V | | 15 | | |
| | $V_I$ = 1.8 V, | $I_O$ = 15 mA | $V_{ref\_A}$ = 3.3 V; $V_{ref\_B} = V_{EN}$ = 5V | | 9.0 | | Ω |
| | $V_I$ = 1.0 V, | $I_O$ = 10 mA | $V_{ref\_A}$ = 1.8 V; $V_{ref\_B} = V_{EN}$ = 3.3V | | 18 | | Ω |
| | $V_I$ = 0V, | $I_O$ = 10 mA | $V_{ref\_A}$ = 1.0 V; $V_{ref\_B} = V_{EN}$ = 3.3V | | 20 | | Ω |
| | $V_I$ = 0V, | $I_O$ = 10 mA | $V_{ref\_A}$ = 1.0 V; $V_{ref\_B} = V_{EN}$ = 1.8V | | 30 | | Ω |

(1) All typical values are at $T_A$ = 25°C.
(2) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

## AC Performance (Translating Down)

### Switching Characteristics

over recommended operating free-air temperature range, $V_{GATE}$ = 3.3 V, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0, and $V_M$ = 1.15 V (unless otherwise noted) (see Figure 8)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 15 pF | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 0 | 0.3 | 0 | 0.2 | 0 | 0.1 | ns |
| $t_{PHL}$ | | | 0 | 0.4 | 0 | 0.3 | 0 | 0.2 | |

### Switching Characteristics

over recommended operating free-air temperature range, $V_{GATE}$ = 2.5 V, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0, and $V_M$ = 0.75 V (unless otherwise noted) (see Figure 8)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 15 pF | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 0 | 0.4 | 0 | 0.3 | 0 | 0.2 | ns |
| $t_{PHL}$ | | | 0 | 0.5 | 0 | 0.4 | 0 | 0.3 | |

## AC Performance (Translating Up)

### Switching Characteristics

over recommended operating free-air temperature range, $V_{GATE}$ = 3.3 V, $V_{IH}$ = 2.3 V, $V_{IL}$ = 0, $V_T$ = 3.3 V, $V_M$ = 1.15 V and $R_L$ = 300 (unless otherwise noted) (see Figure 8)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 15 pF | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 0 | 0.3 | 0 | 0.2 | 0 | 0.1 | ns |
| $t_{PHL}$ | | | 0 | 0.4 | 0 | 0.3 | 0 | 0.2 | |

### Switching Characteristics

over recommended operating free-air temperature range, $V_{GATE}$ = 2.5 V, $V_{IH}$ = 1.5 V, $V_{IL}$ = 0, $V_T$ = 2.5 V, $V_M$ = 0.75 V and $R_L$ = 300 (unless otherwise noted) (see Figure 8)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 15 pF | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 0 | 0.4 | 0 | 0.3 | 0 | 0.2 | ns |
| $t_{PHL}$ | | | 0 | 0.5 | 0 | 0.4 | 0 | 0.3 | |

## APPLICATION INFORMATION

The LSF0101/2 can be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The LSF0101/2 is ideal for use in applications where an open-drain driver or push-pull is connected to the data I/Os.

### Enable, Disable and Reference Voltage Guide

The LSF0101/2 has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF0101/2 is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF0101/2 for bidirectional application, like I2C, SMBus, PMBus, MDIO.

| APPLICATION OPERATING CONDITION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
| Vref_A | reference voltage (A) | 1 | | 4.5 | V |
| Vref_B | reference voltage (B) | Vref_A + 0.8 | | 5.5 | V |
| $V_{I(EN)}$ | input voltage on EN pin | Vref_A + 0.8 | | 5.5 | V |
| Vpu | pull-up supply voltage | 0 | | Vref_B | V |

**The 200kΩ, pull-up resistor is required to allow Vref_B to regulate the EN input.** A filter capacitor on Vref_B is recommended. Also Vref_B and $V_{I(EN)}$ are recommended to be at 1.0 V higher than Vref_A for best signal integrity.

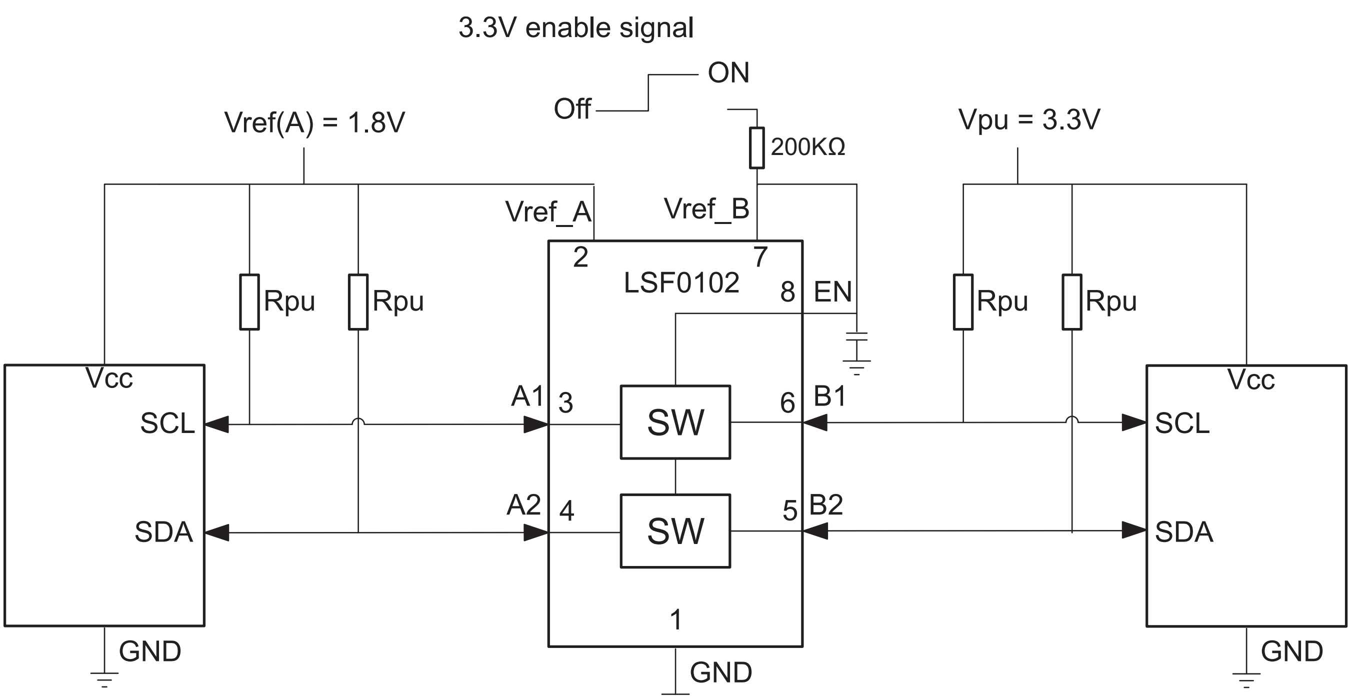



**Figure 7.**

## Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to Vref_B and both pins pulled to HIGH side Vpu through a pull-up resistor (typically 200kΩ). This allows Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. The master output driver can be push-pull or open-drain (pull-up resistors may be required) and the slave device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

**However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.**

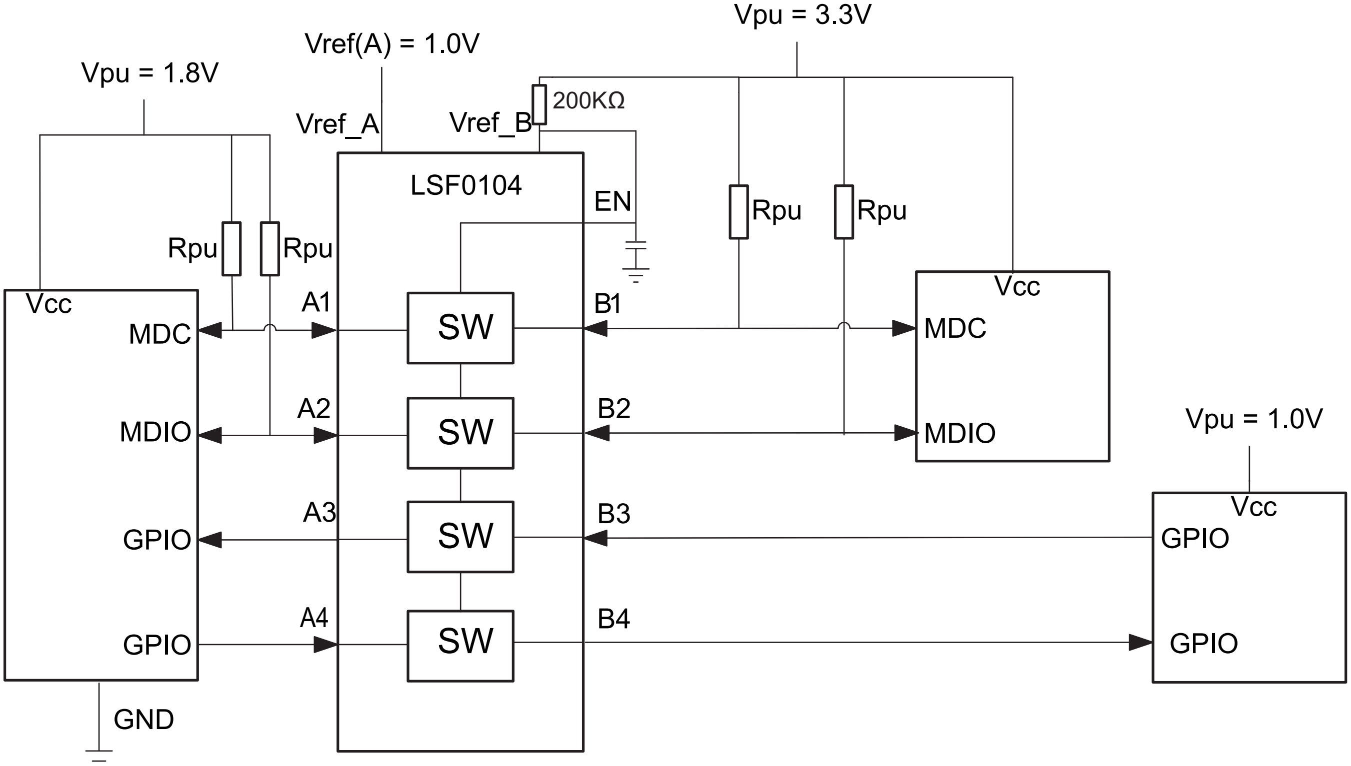



**Figure 8.**

In the above figure, the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through a 200 kΩ resistor to a 3.3 V Vpu power supply, and Vref_A is set 1.0V. The output of A3 and B4 has a maximum output voltage equal to Vref_A, and the bidirectional interface (Ch1/2, MDIO) has a maximum output voltage equal to Vpu.

## Pull-up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, to calculate the pull-up resistor value use the following equation:

Rpu = (Vpu – 0.35V) / 0.015A

Table 1 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF0101/2 device at 0.175 V, although the 15 mA applies only to current flowing through the LSF0101/2 device.

**Table 1. Pull-up Resistor Values(1)(2)**

| | PULL-UP RESISTOR VALUE (Ω) | | | | | |
|---|---|---|---|---|---|---|
| $V_{DPU}$ | 15 mA | | 10 mA | | 3 mA | |
| | NOMINAL | +10% (3) | NOMINAL | +10% (3) | NOMINAL | +10% (3) |
| 5 V | 310 | 341 | 465 | 512 | 1550 | 1705 |
| 3.3 V | 197 | 217 | 295 | 325 | 983 | 1082 |
| 2.5 V | 143 | 158 | 215 | 237 | 717 | 788 |
| 1.8 V | 97 | 106 | 145 | 160 | 483 | 532 |
| 1.5 V | 77 | 85 | 115 | 127 | 383 | 422 |
| 1.2 V | 57 | 63 | 85 | 94 | 283 | 312 |

(1) Calculated for $V_{OL}$ = 0.35 V
(2) Assumes output driver $V_{OL}$ = 0.175 V at stated current
(3) +10% to compensate for $V_{DD}$ range and resistor tolerance

## LSF0101/2 Bandwidth

The maximum frequency of the LSF0101/2 is dependent on the application. The device can operate at speeds of >100MHz gave the correct conditions. The maximum frequency is dependent upon the loading of the application. The LSF0101/2 behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

Figure 9 shows a bandwidth measurement of the LSF0101/2 using a two-port network analyzer.

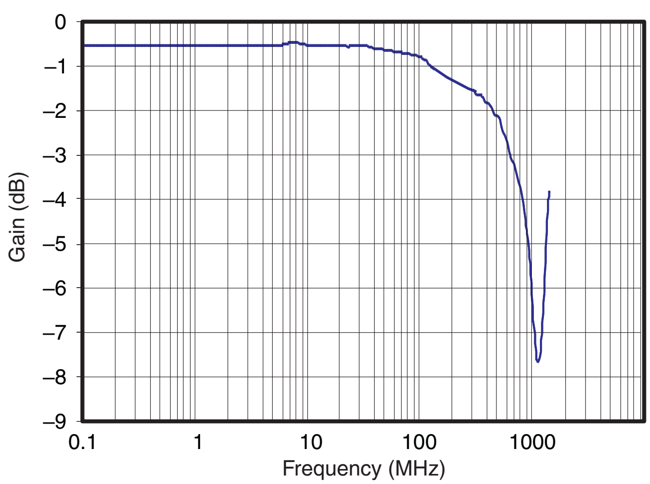



**Figure 9. 3dB Bandwidth**

The 3-dB point of the LSF0101/2 is ≈600MHz; however, this measurement is an analog type of measurement. For digital applications the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the LSF0101/2, a digital clock frequency of greater than 100 MHz can be achieved.

The LSF0101/2 does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pull-up resistor is needed on the host side (3.3 V) if the LSF0101/2 is being driven by standard CMOS totem pole output driver. Ideally, it is best to minimize the trace length from the LSF0101/2 on the sink side (1.8 V) to minimize signal degradation.

All fast edges have an infinite spectrum of frequency components; however, there is an inflection (or "knee") in the frequency spectrum of fast edges where frequency components higher than $f_{knee}$ are insignificant in determining the shape of the signal.

To calculate the maximum "practical" frequency component, or the "knee" frequency ($f_{knee}$), use the following equations:

$f_{knee}$ = 0.5/RT (10–80%)

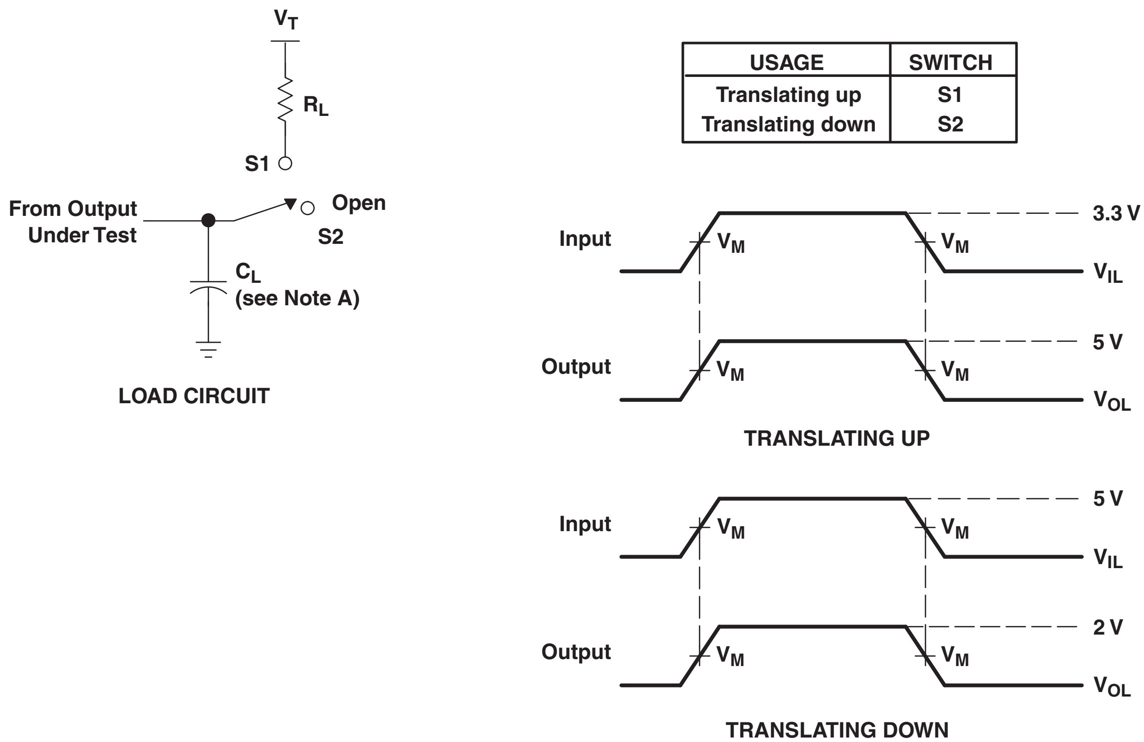
$f_{knee}$ = 0.4/RT (20–80%)

For signals with rise time characteristics based on 10- to 90-percent thresholds, $f_{knee}$ is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20% to 80% thresholds, which is very common in many of today's device specifications, $f_{knee}$ is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the LSF0101/2 close to the $I^2C$ output of the processor
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region
- To reduce overshoots, a pul-lup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected

## Parameter Measurement Information




NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

**Figure 10. Load Circuit for Outputs**

## REVISION HISTORY

| Changes from Original (December 2013) to Revision A | Page |
|---|---|
| • Updated part number. | 1 |
| • Updated Signal Integrity (1.8V to 3.3V Translation Up at 50 MHz) graphic. | 3 |
| • Updated Electrical Characteristics table. | 6 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LSF0101DRYR | ACTIVE | SON | DRY | 6 | 5000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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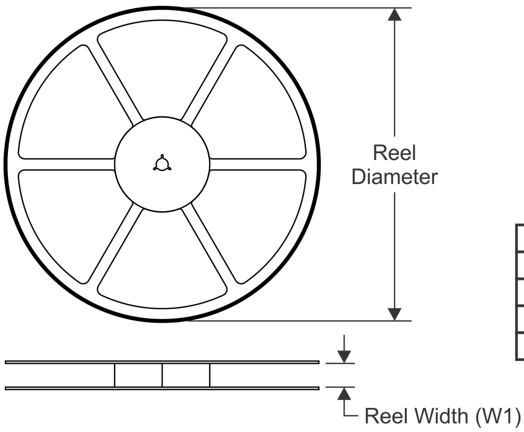
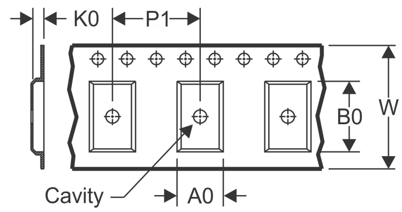
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

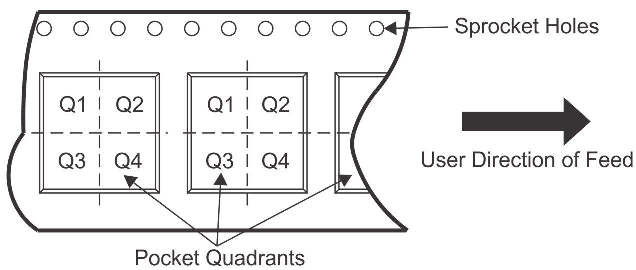



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

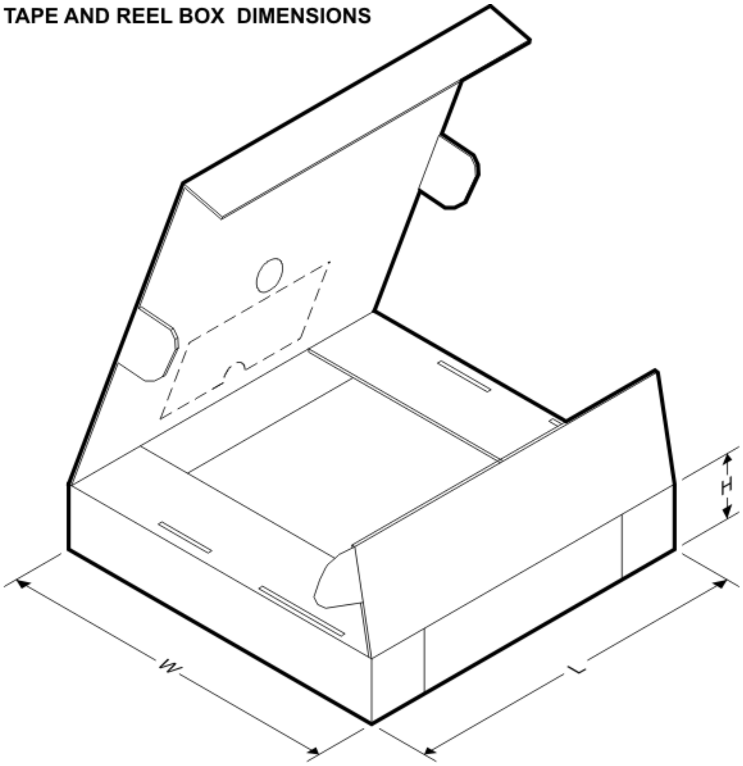
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LSF0101DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |

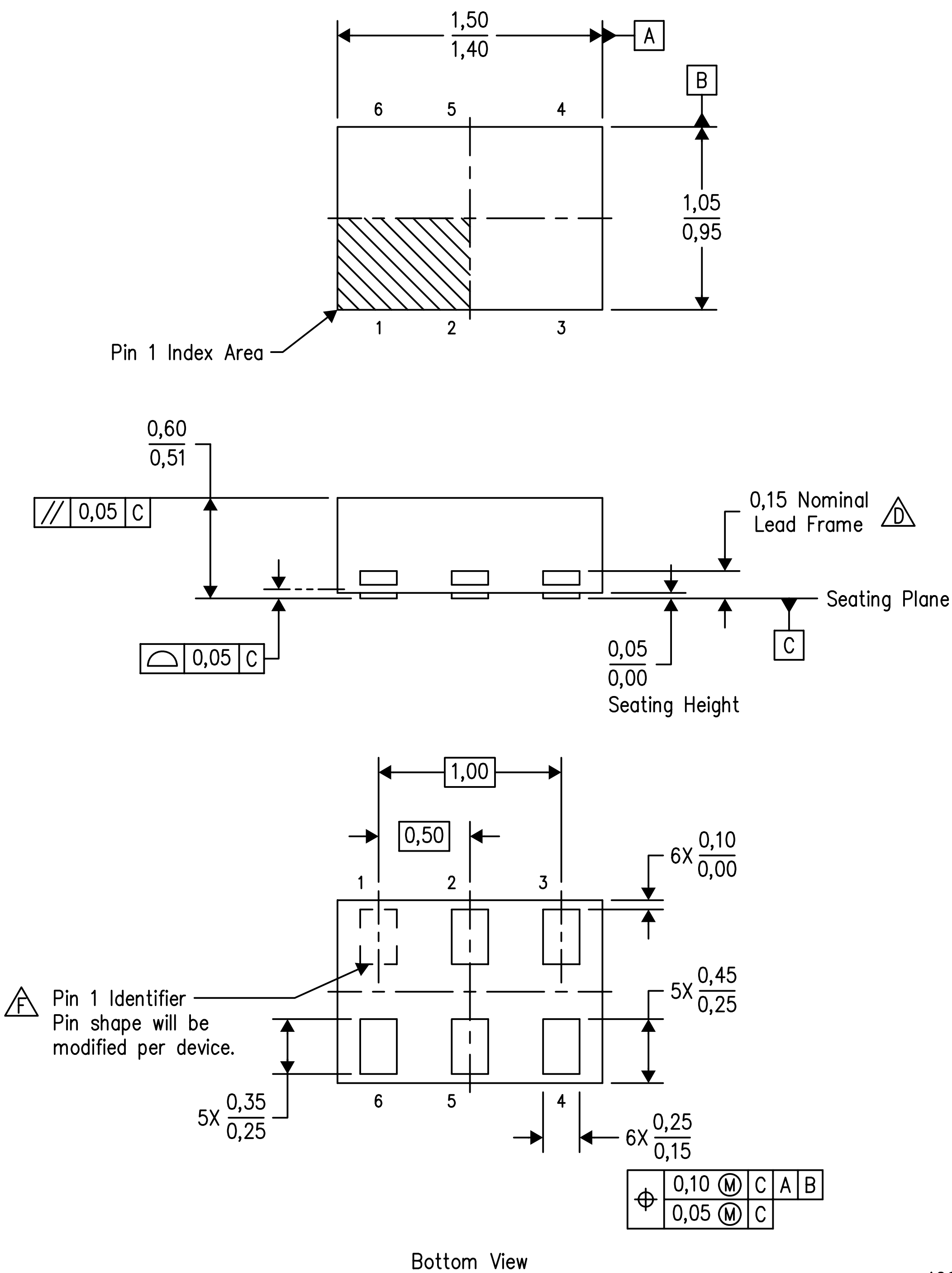
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LSF0101DRYR | SON | DRY | 6 | 5000 | 180.0 | 180.0 | 30.0 |

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

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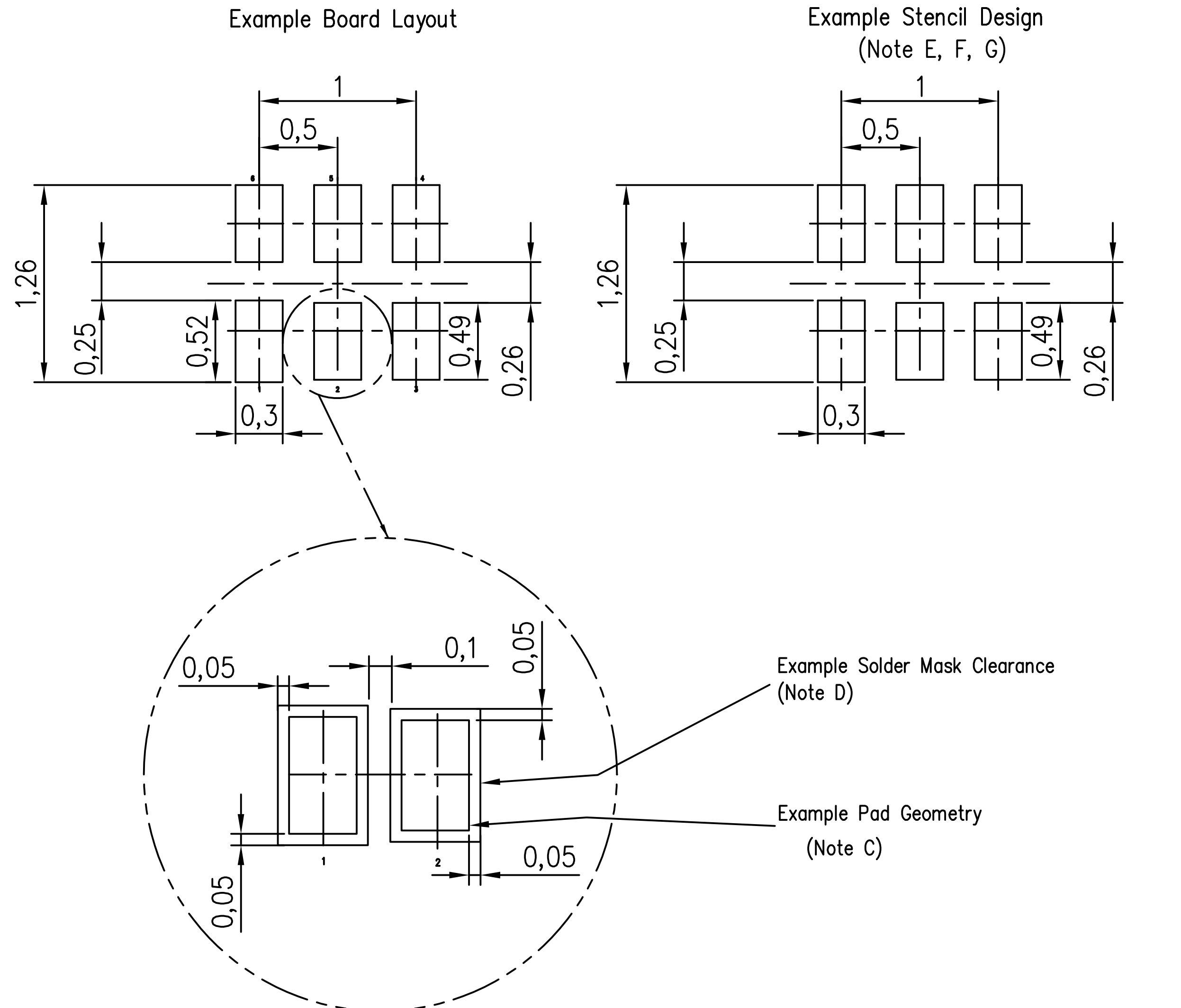
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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